REMARKS

Applicants have studied the Office Action dated July 31, 2003 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-23 and 30-38 are pending. Claims 1, 4, 7, 8, 11, 14, 15, 18-20, and 23 have been amended, and new claims 35-38 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

Claims 1, 2, 4, and 30-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sandhu et al. (U.S. Patent No. 5,959,327) in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publications, pp. 157, 868). Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al. and Rhodes et al. (U.S. Patent No. 6,492,241). Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al. and Maeda (U.S. Patent No. 6,358,820). Claims 7-9, 11-13, 19-23, 33, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., Sung et al. (U.S. Patent No. 6,133,599) and Trivedi (U.S. Patent No. 6,294,464). Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., Sung et al., Trivedi, and Maeda. Claims 14-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., Sung et al., Rhodes et al., and Trivedi. These rejections are respectfully traversed.

The present invention is directed to providing an easy to manufacture electrical contact having a low-resistance for contacting a passive component and another component of an integrated circuit. One embodiment provides an integrated circuit having a plurality of active components and at least one passive component situated above the active components. The integrated circuit includes a first insulating layer that separates the active components and a base

of the passive component, and a metal terminal that electrically connects the passive component with at least one of the active components.

The metal terminal is formed in the thickness of the first insulating layer, has a lower surface that contacts a junction of the one active component such that the lower surface of the metal terminal extends over a boundary of the junction of the one active component, and has an upper surface that contacts the base of the passive component. The metal terminal consists of a single layer of metal that extends from the junction of the one active component to the base of the passive component. Because the metal terminal consists of a single layer of metal extending from the active component to the passive component, the terminal is easy to manufacture while providing a low electrical resistance. Additionally, because the lower surface of this metal terminal extends over the boundary of the junction of the active component, the contact resistance is reduced and dopant atoms are prevented from penetrating as far as the junction of the active component.

The Sandhu reference discloses a dynamic random access memory device that includes a storage cell capacitor with a storage node having a barrier layer that prohibits diffusion of atoms. However, Sandhu does not disclose an integrated circuit having active components and at least one passive component that includes a first insulating layer separating the active components and a base of the passive component, and a metal terminal having a lower surface that contacts a junction of one of the active components and an upper surface that contacts the base of the passive component, with the metal terminal consisting of a single layer of metal extending from the junction of the one active component to the base of the passive component, as is recited in amended claim 1.

Likewise, Sandhu does not disclose an integrated circuit including transistors, passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors, with the integrated circuit including a first metal terminal constituting a first stage of contact between one active area of the integrated circuit and a first level of interconnection, and having an upper surface that contacts a second stage of such contact, a second metal terminal vertically connecting one active area of the integrated circuit to

a passive component, and a third metal terminal horizontally connecting two separate active areas of the integrated circuit, with the first metal terminal consisting of a single layer of metal extending from the one active area of the integrated circuit to the second stage of contact, and the third metal terminal consists of a single layer of metal., as is recited in amended claim 7. Amended claims 14 and 19 contain similar recitations.

The memory device disclosed in Sandhu includes a transistor 22 that is associated with a capacitor 85-90-95, as shown in Figure 13A. The transistor 22 has one junction 30 that is electrically connected to one plate 85 of the capacitor by a plug 65-67-75. This connecting plug is composed of a lower layer of polycrystalline silicon 65, an intermediate layer of titanium silicide 67, and an upper layer of titanium nitride 75. Thus, Sandhu teaches electrically connecting the junction of the transistor to the capacitor by using a composite plug that is made partly of polysilicon and partly of metal silicide and metal nitride.

In contrast, in the embodiment of the present invention recited in amended claim 1, the metal terminal for electrically connecting the junction of the active component to the passive component consists of a single layer of metal that extends from its lower surface, which contacts the junction of the active component, to its upper surface, which contacts the base of the passive component. For example, in the exemplary embodiment shown in Figures 5 and 6, a metal terminal 107 provides a vertical electrical connection between a transistor T in an active area 109 and a capacitor C. This metal terminal 107 has a lower surface that contacts one of the junctions 104 of the transistor T, and has an upper surface that contacts the bottom electrode 126 of the capacitor C. Further, the metal terminal 107 is formed of a single layer of metal (for example, tungsten) from the lower surface to the upper surface.

Thus, in this embodiment of the present invention, the metal terminal for electrically connecting the junction of the active component to the passive component is made of metal and does not have multiple layers. Because the metal terminal consists of a single layer of metal, the terminal is easy to manufacture while providing a low electrical resistance. Further, because the terminal used to make this electrical contact is made of a metal such as tungsten, the many

drawbacks of using polysilicon for this contact are avoided. For example, using polysilicon causes problems regarding ohmic contact between the polysilicon 18 and the doped monocrystalline silicon region 6a, and also results in low contact efficiency because the quality of the monocrystalline silicon/polycrystalline silicon interface is difficult to control and make reproducible. See specification at 4:7-17; Fig. 2.

Additionally, the use of a tungsten terminal creates a barrier to diffusion so that phosphorus atoms from the polycrystalline layer 126 cannot penetrate the junction of region 104 of the transistor T. This, in turn, allows use of an atom that diffuses easily with a reduced thermal budget. For example, with the use of the claimed structure, it is possible to perform phosphorus implantation followed by rapid thermal annealing (for example, for 20 seconds at 1,000°C, as opposed to 950°C for 20 minutes when polysilicon is used). See specification at 12:11-23.

Neither Sandhu nor Wilson, or a combination of the two, teaches or suggests a metal terminal for electrically connecting the junction of an active component to a passive component that has a lower surface that contacts the junction such that the lower surface extends over a boundary of the junction, and that consists of a single layer of metal extending from the junction of the active component to the base of the passive component. Sandhu teaches using a composite plug that is made partly of polysilicon and partly of metal silicide and metal nitride. Wilson only generally teaches that tungsten plugs can be used for making electrical connections.

Applicants respectfully submit that generally knowing that metal plugs can be used to make electrical interconnections would not have made it obvious to one of ordinary skill in the art to use a plug made entirely of a single layer of metal with a lower surface extending over a boundary of the junction of an active component in the recited type of device. There is absolutely no teaching or suggestion in Wilson to use such a metal terminal to connect the junction of an active component to a passive component. Likewise, there is no teaching or suggestion in Sandhu of replacing the disclosed multiple layer composite plug with a single layer metal terminal so as to provide the advantages of the present invention. These claimed features of a metal terminal having a lower surface that extends over a boundary of the junction and

consisting of a single layer of metal allow the present invention to provide an easy to manufacture electrical contact that has a low resistance and provides many other advantageous.

Furthermore, as recognized by the Examiner, Sandhu does not disclose the first metal terminal and third metal terminal recited in amended claims 7, 14, and 19. However, the Examiner went on to take the position that Sandhu and Wilson teach the recited second metal terminal and that Sung and Trivedi make up for the deficiency in the disclosure of Sandhu. This position of the Examiner is respectfully traversed.

First, for at least the reasons explained above, Applicants respectfully submit that neither Sandhu nor Wilson, or a combination of the two, teaches or suggests the second metal terminal for vertically connecting one active area of the integrated circuit to a passive component that directly contacts the upper surface of a first insulating layer.

Additionally, the Sung reference discloses a DRAM device having plugs 16b and 17b made of polysilicon that pass through the thickness of an insulating layer 11. A capacitor is electrically connected to a junction of a transistor through the first polysilicon plug 16b, as shown in Figure 9. A tungsten plug 24 contacts the second polysilicon plug 17b for connecting to another junction of the transistor. Thus, in the device of Sung, polysilicon plus are used as contacts through the insulating layer.

In contrast, in the embodiment of the present invention recited in amended claims 7, 14, and 19, the second terminal is a metal terminal and the first terminal consists of a single layer of metal that extends from the active area to a second stage of contact between the active area and a first level of interconnection. Sung only teaches using a polysilicon plug to contact with the junction of the transistor through the insulating layer, and does not teach or suggest using a metal terminal consisting of a single layer of metal. As explained in detail above, the use of polysilicon to contact the active area of a transistor causes problems regarding ohmic contact, which is clearly undesirable. The use of a metal terminal consisting of a single layer of metal allows the

present invention to provide an easy to manufacture electrical contact that has a low resistance and provides many other advantageous (as explained above).

Further, the Trivedi reference discloses a DRAM device having a local interconnection in a horizontal plane provided by a horizontal plug 37, as shown in Figure 7. This horizontal plug 37 is made of a composite structure based on silicon and tungsten. Because the plug of Trivedi has this type of composite structure, Applicants do not understand how it would be possible to constitute a single insulating layer containing the three types of plugs that are obtained when the plugs disclosed in Sandhu, Sung, and Trivedi are combined.

In contrast, in the embodiment of the present invention recited in amended claims 7, 14, and 19, the recited first, second and third metal terminals are provided so as to completely pass through a single insulating layer. Further, Trivedi does not teach or suggest the use of the disclosed horizontal plug for providing the recited interconnections in a device having active and passive components arranged in the recited manner.

Furthermore, Applicants submit that it is improper to combine these four references to each show an individual feature of the claimed invention. First, none of the references even teaches or suggests one of the recited limitations. The Examiner uses a different reference to assert that each of the recited limitations is obvious, but none of these references even teaches or suggests its corresponding limitation. Each reference must be combined with Wilson just to assert that the corresponding limitation is obvious. The use of different references for each claim limitation, especially when none of these references actually teaches or suggests its corresponding limitation, demonstrates that the combination of claimed features is not obvious.

Additionally, even if each of Sandhu, Sung, and Trivedi suggest one of the recited terminals of the claimed integrated circuit, there is no teaching or suggestion to simultaneously use three such metal terminals in a single insulating layer of a device. Even if each reference suggests one claimed feature, the Examiner has not cited any reference or generally available knowledge that suggests or provides any motivation for combining three such features and the

general knowledge of Wilson so as to produce the claimed integrated circuit structure having the three specific metal terminals in a single insulating layer of a device as is recited.

Nearly all integrated circuit structures include the same basic elements and features (such as conducting lines and regions, insulating layers and regions, semiconductor regions, doped regions, an contacts) combined in different manners with very different results. If all that was required to sustain a finding of obviousness was that each separate feature of an integrated circuit structure was disclosed in some other integrated circuit structure, then few (if any) integrated circuit structure patents would be issuing at this time. However, a great number of such patents continue to issue because this is certainly not the law and there must be shown some specific motivation for combining a feature found in one reference in a specific manner into a different type of circuit structure found in another reference in order to sustain a finding of obviousness.

Here, the specific arrangement of the three metal terminals in the first insulating layer makes it possible to realize all the necessary connections within the first insulating layer in a simultaneous manner with a reduced number of operations, plus all of the individual advantages described above. Thus, besides providing easy to manufacture and low resistance contacts, all of the interconnections in the first insulating layer are formed at the beginning of the manufacturing process.

Additionally, an individual element found in one reference cannot simply be substituted into a different type of circuit structure in another reference with the same results. Even a small change in the type and placement of a specific element or feature in relation to other elements and features can produce very different and unexpected results. None of the cited references provides any suggestion or motivation for forming the three metal terminals in the first insulating layer as recited.

The cited references fail to meet the basic requirement for a finding of obviousness established by the courts. There is simply no suggestion or motivation in any of these references for combining selected features of one reference with the integrated circuit structure of the other reference in order to produce a single integrated circuit structure, nor is there any suggestion of the desirability of such a combination. Without Applicants' specification, there would be no suggestion or motivation to one of ordinary skill in the art at the time of the invention to produce

the recited structure. It is respectfully submitted that the Examiner is engaging in hindsight reconstruction of the claimed invention.

Furthermore, the claimed features of the present invention are not realized even if the teachings of Rhodes are incorporated into Sandhu, Wilson, Sung, and Trivedi. Rhodes does not teach or suggest the claimed features of the present invention that are absent from Sandhu, Wilson, Sung, and Trivedi.

Applicants believe that the differences between Sandhu, Wilson, Sung, Trivedi, Rhodes, and the present invention are clear in amended claims 1, 7, 14, and 19, which set forth various embodiments of the present invention. Therefore, claims 1, 7, 14, and 19 distinguish over the Sandhu, Wilson, Sung, Trivedi, and Rhodes references, and the rejections of these claims under 35 U.S.C. § 103(a) should be withdrawn.

As discussed above, claims 1, 7, 14, and 19 distinguish over the Sandhu, Wilson, Sung, Trivedi, and Rhodes references. Furthermore, the claimed features of the present invention are not realized even if the teachings of Maeda are incorporated into Sandhu, Wilson, Sung, Trivedi, and Rhodes. Maeda does not teach or suggest the claimed features of the present invention that are absent from Sandhu, Wilson, Sung, Trivedi, and Rhodes. Thus, claims 1, 7, 14, and 19 distinguish over the Sandhu, Wilson, Sung, Trivedi, Rhodes, and Maeda references, and thus, claims 2-6 and 30-32, claims 8-13, 33, and 34, claims 15-18, and claims 20-23 (which depend from claims 1, 7, 14, and 19, respectively) also distinguish over the Sandhu, Wilson, Sung, Trivedi, Rhodes, and Maeda references. Therefore, it is respectfully submitted that the rejections of claims 1-23 and 30-34 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 35-38 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 35-38 are allowable for at least the reasons set forth above with respect to claims 1-23 and 30-34.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

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